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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,434	12/03/2003	Toshihiko Iinuma	04329.3189	5328

22852 7590 08/19/2005

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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,434	IINUMA, TOSHIHIKO	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1A – 1F, 2A-2g, and 3A-3E should be designated by a legend such as --Prior Art-- because the applicant admits that these drawings illustrate the conventional method of manufacturing a MOS type FET device where the nickel silicide process has been employed, which illustrates only that which is old. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-7, and 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art in view of Yamazaki et al. (USPN 6589829 B2), Paton et al. (USPN 6797614 B1) and Skee (USPN 6,599,370).

See applicant's specification for admitted prior art. Applicant discloses a conventional method of manufacturing a MOS type FET device (p.3, l.12-13) which has been conducted by forming a diffusion region (fig. 1A, 105) that includes: an implanted impurity (p.3, l. 22-23) in the diffusion region (written on element region) (p.3, l.24) of a silicon substrate (fig. 1A, 101) that is isolated by an insulator (fig. 1A, 102) with a gate electrode (fig. 1A, 104) formed over a gate insulating film (fig. 1A, 103) with the element isolating insulating film (fig. 1A, 102) preventing the nickel film (fig. 1A, 108) from taking part in the reaction with the silicon (pg. 4, 1.19 is written on being employed as a mask). Applicant's admitted prior art discloses depositing nickel metal (fig. 1C, 108) over the

entire top surface (p.4, l.7) of the silicon substrate (fig. 1C, 101); a heat treatment which forms NiSi (fig. 1D, 109) , and is conducted at 450 degree C or more, for not more than 5 min (p.4 l.10); removing any unreacted portion (p.4, l.22) of nickel metal deposited (fig. 1E, 108) from element isolating insulation film (fig. 1E, 102). Applicant's admitted prior art discloses depositing an interlayer insulating film (fig. 1E, 110) over the entire top surface of said silicon substrate (fig. 1E, 101); and subjecting to RIE (p.5, l.5-6) to form a wiring layer (fig.1F, 111) which pierces through the interlayer insulating film (fig. 1F, 110).

Applicant's admitted prior art does not disclose: the concentration of the arsenic implant at a concentration of 1.times.10.sup.20 cm.sup.-3 or more; and the use of a second heat treatment, at less than 400 degree C. which forms Ni2Si , the higher temperature heat treatment preformed after unreacted metal is removed, and the removal of surface arsenic by use of an alkaline liquid.

Yamazaki et al. teaches use of conventional intergrate circuit producing technique (col.6, l-49-50) wherein impurity regions were formed, with self-alignment, using the field insolating members and the gate electrodes as masks. Embodiment 1, discusses an element region containing arsenic impurities of $1x10^{20}$ cm^{-3} (col.6, l.60-64), as claimed by the instant application.

Yamazaki et al. also teaches the use of a second heat treatment, at less than 400 degree C. which forms Ni2Si , the higher temperature heat treatment preformed after unreacted metal is removed, and the removal of surface arsenic by use of an alkaline liquid.

It would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the conventional method of manufacturing a MOS type FET device, of applicants admitted prior art, by forming impurity regions with self-alignment, using the field insolating members and the gate electrodes as masks, of Yamazaki et al., because Yamazaki and the applicant both teach such methods and techniques are conventional and lower electric resistance capable of suppressing the generation of the junction leak.

Paton teaches a salicide process that is advantageous for improved stability and suitable resistance for silicide regions on the IC substrate (col.3, l.23-25). Paton teaches use the following flow (see fig. 2) for a nickel silicide process: form the gate structure(col.6, l.15); providing a nickel alloy layer (col.6, l.16); anneal with nitride to form nickel disilicide, preferably at 320-400.degree, at the claimed temperature of less than 400, in a nitrogen ambient (col.6, l.21-23); nickel alloy which is not silicided is stripped (col.6, l.24); the remaining partion is annealed for a second time, and changes dinickel suicide into mononickel silicide, at a temperature of 400-600.degree C., encompassing the claimed temperature of 450 degree C or more, in a nitrogen ambient (col.6, l.26-31); and unreacted nickel alloy can be stripped again (col.6, l.33). Patton teaches this silicidation is less likely to cause shorts across spacer, and can be further improved by implanting a portion of the substrate with silicon prior to silicidation (col.6, l.35-40).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the conventional method of manufacturing a MOS type

FET device, of applicants admitted prior art, by forming impurity regions with self-alignment, using the field insolating members and the gate electrodes as masks, of Yamazaki et al., and then combining it with the salicide process of Paton et al., because Paton teaches it advantageously improves stability with suitable resistance for silicide regions on the IC substrate.

Skee teaches removal of organic and inorganic compositions from substrates without damaging the integrated circuits (col.4, l.6-9, is written on the removal of surface arsenic compound). Skee's compositions include hydrogen peroxide (col.4, l.37), ammonium (col.4, l.30-31 writtten on ammonia), choline (col.5, l.51), and are aqueous, alkaline, stripping and cleaning compositions (col.6, l.31-32). Skee teaches such compositions remove unwanted contaminants and/or residues from the substrate surface (col.4, l.16-20).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the conventional method of manufacturing a MOS type FET device, of applicants admitted prior art, by forming impurity regions with self-alignment, using the field insolating members and the gate electrodes as masks, of Yamazaki et al., with the silicide process of Paton et al., and removal method of metallic and organic contamination from such substrates without damaging the integrated circuits, of Skee, because Skee teaches such compositions remove unwanted contaminants and/or residues from the substrate surface, as to claims 1 and10.

As for claims 2 and 12, an alkaline liquid comprising a mixed solution containing aqueous ammonia and aqueous hydrogen peroxide, see discussion of Skee's compositions above.

As for claims 3 and 13, an alkaline liquid of a mixed solution containing choline and aqueous hydrogen peroxide, see discussion of Skee's compositions above.

As for claims 4 and 14, a temperature of the first heat treatment is 250.degree. C. or more, see discussion on Paton's silicide process above.

As for claim 5 and 15, a temperature of the second heat treatment is 550.degree. C. or less, see discussion on Paton's silicide process above.

As for claims 6 –7 and 16-17, a heat-treating of first and second temperatures are performed for a period of less than five minutes, see the time claimed for the heat treatment of the applicants admitted prior art above.

As for claim 11, wherein said metal film is a nickel film, said first metal silicide is di-nickel silicide (Ni.sub.2Si), and said second metal silicide is nickel monosilicide (NiSi), see discussion on Paton above.

Claim Rejections - 35 USC § 103

Claims 8-9 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art and Yamazaki et al., Paton et al., and Skee, of claims 1-7, and 10-17 above, in further view of Einav (USPN 6720617).

As for claims 8-9 and 18-19, Einav teaches a method of manufacture a FET-structure, all operations being low temperature operations, performed in high vacuum

chambers, including insulator substrates and semiconductor and/or metal (col.3, 25-29), at a temperature of 25-250 degree. C, (col.7, l.3), well within the claimed limitations of 500 degree. C. or 550.degree. C. or less. Eivan teaches the technique enables to obtain the width-to-length ratio about 100, which results in the significant reduction of the voltage supply (col.7, l.9–14).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the conventional method of manufacturing a MOS type FET device, of applicants admitted prior art, Yamazaki et al., Paton et al., and Skee, with the low temperature depositions for the insulator and metal wires, because Eivan teaches a significant reduction of the voltage supply.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Du Pont Products Sheet; 2004; E.I. DuPont de Numerous and Company;

Ceria Slurries: Altrnative Slurry for Post CMP Cleans; Maria A. lester, Associate Editor -- Semiconductor International, May 1, 2002.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patricia A George
Examiner
Art Unit 1765

PAG
07/05

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER